IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A semiconductor structure having a dielectric layer, comprising:

a conductive container structure having a closed bottom and sidewalls extending upward from the closed bottom; and

a dielectric cap on a top of the sidewalls, wherein the dielectric cap is adapted to remain on the top of the sidewalls and form part of the dielectric layer, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides and silicon oxynitrides.

2. (Original) The semiconductor structure of claim 1, wherein the conductive container structure has a cylindrical shape.

3. (Original) The semiconductor structure of claim 1, wherein the closed bottom and sidewalls comprise at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.

4. (Original) The semiconductor structure of claim 3, wherein the at least one silicon material is conductively doped.

5. (Canceled)

6. (Currently Amended) A semiconductor structure having a dielectric layer, comprising:

a conductive container structure having a closed bottom and sidewalls extending upward from the closed bottom, wherein the closed bottom and sidewalls comprise at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon; and

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides~~, nitrides~~ and silicon oxynitrides, and wherein the dielectric cap is adapted to remain on the top of the sidewalls and form part of the dielectric layer.

7. (Original) The semiconductor structure of claim 6, wherein the dielectric cap is annealed.

8. (Previously Presented) A semiconductor structure having a dielectric layer, comprising:

a conductive container structure having sidewalls, wherein the conductive container structure comprises conductively-doped hemispherical grain polysilicon; and

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride, wherein the dielectric cap is adapted to remain on the top of the sidewalls and form part of the dielectric layer.

9. (Original) The semiconductor structure of claim 8, wherein the dielectric cap is annealed at approximately 600 °C to 1000 °C for approximately 10 to 20 seconds.

10.-52. (Canceled)

53. (Currently Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides and silicon oxynitrides;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

54. (Original) The semiconductor die of claim 53, wherein the bottom plate has a cylindrical shape.

55. (Original) The semiconductor die of claim 53, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.

56. (Original) The semiconductor die of claim 55, wherein the at least one silicon material is conductively doped.

57. (Canceled)

58. (Original) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

59. (Original) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises conductively-doped hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

60. (Original) The semiconductor die of claim 43, wherein the dielectric cap is annealed at approximately 600 °C to 1000 °C for approximately 10 to 20 seconds.

61-68. (Canceled)

69. (Original) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom;

a dielectric cap on a top of the sidewalls;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

70. (Original) The memory device of claim 69, wherein the bottom plate has a cylindrical shape.

71. (Original) The memory device of claim 69, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.

72. (Original) The memory device of claim 71, wherein the at least one silicon material is conductively doped.

73. (Original) The memory device of claim 69, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

74. (Original) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

75. (Original) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises conductively-doped hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

76. (Original) The memory device of claim 75, wherein the dielectric cap is annealed at approximately 600 °C to 1000 °C for approximately 10 to 20 seconds.

77.-84. (Canceled)

85. (Original) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom;

a dielectric cap on a top of the sidewalls;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

86. (Original) The memory module of claim 85, wherein the bottom plate has a cylindrical shape.

87. (Original) The memory module of claim 85, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.

88. (Original) The memory module of claim 87, wherein the at least one silicon material is conductively doped.

89. (Original) The memory module of claim 85, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

90. (Original) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

91. (Original) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises conductively-doped hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

92. (Original) The memory module of claim 91, wherein the dielectric cap is annealed at approximately 600 °C to 1000 °C for approximately 10 to 20 seconds.

93. (Original) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom;

a dielectric cap on a top of the sidewalls;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

94. (Original) The memory system of claim 93, wherein the bottom plate has a cylindrical shape.

95. (Original) The memory system of claim 93, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.

96. (Original) The memory system of claim 95, wherein the at least one silicon material is conductively doped.

97. (Original) The memory system of claim 93, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

98. (Original) A memory system, comprising:
a controller;
a command link coupled to the controller;
a data link coupled to the controller; and
a memory device coupled to the command link and the data link, wherein the memory device comprises:
an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:
a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;
a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

99. (Original) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises conductively-doped hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

100. (Original) The memory system of claim 99, wherein the dielectric cap is annealed at approximately 600 °C to 1000 °C for approximately 10 to 20 seconds.

101. (Original) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom;

a dielectric cap on a top of the sidewalls;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

102. (Original) The electronic system of claim 101, wherein the bottom plate has a cylindrical shape.

103. (Original) The electronic system of claim 101, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon.

104. (Original) The electronic system of claim 103, wherein the at least one silicon material is conductively doped.

105. (Original) The electronic system of claim 101, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

106. (Original) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

107. (Original) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices is a container capacitor, the container capacitor comprising:

a bottom plate having a closed bottom and sidewalls extending upward from the closed bottom, wherein the bottom plate comprises conductively-doped hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride;

a dielectric layer on the bottom plate and the dielectric cap; and

a cell plate on the dielectric layer, wherein the dielectric layer is interposed between the cell plate and the bottom plate.

108. (Original) The electronic system of claim 107, wherein the dielectric cap is annealed at approximately 600 °C to 1000 °C for approximately 10 to 20 seconds.

109.-124. (Canceled)

125. (Currently Amended) A semiconductor structure, comprising:

a conductive container structure having a closed bottom and sidewalls extending upward from the closed bottom;

~~a~~ an oxide dielectric cap on a top of the sidewalls; and

a dielectric layer on the dielectric cap and the conductive container structure.

126. (Currently Amended) A semiconductor structure, comprising:

a conductive container structure having a closed bottom and sidewalls extending upward from the closed bottom, wherein the closed bottom and sidewalls comprise at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of silicon oxides~~, nitrides~~ and silicon oxynitrides; and

a dielectric layer on the dielectric cap and the conductive container structure.

127. (Previously Presented) A semiconductor structure, comprising:

a conductive container structure having sidewalls, wherein the conductive container structure comprises conductively-doped hemispherical grain polysilicon;

a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises silicon oxynitride; and

a dielectric layer on the dielectric cap and the conductive container structure.